Claims

1. An integrated circuit semiconductor memory device comprising:

a substrate;

a first dielectric layer covering a first portion of said substrate, said first dielectric layer being absent from a second portion of said substrate;

a second dielectric layer having a property different from said first dielectric layer, said second dielectric layer at least partly covering said second portion of said substrate;

a source region formed in a first doped region on said first dielectric layer;

a drain region formed in a second doped region on said first dielectric layer; and

a gate formed over said second dielectric layer and between said first and second doped regions,

wherein said property of said second dielectric layer provides a gate capacitance of said gate with respect to said substrate that is greater than a theoretical capacitance of a gate formed over said first dielectric layer on said substrate.

2. The device of claim 1, wherein said device is RAM.

3. The device of claim 1, wherein said device is SRAM.

4. The device of claim 1, wherein said device includes a FET.

5. The device of claim 4, wherein said FET is a FinFET.

6. The device of claim 5, wherein said first dielectric layer is a buried oxide layer and said second dielectric layer is a thin oxide layer providing less insulating effect than said buried oxide layer, said gate being capacitively coupled to

said substrate.

7. The device of claim 6, wherein a fin of said FinFET is formed over said buried oxide layer.

8. The device of claim 5, wherein said device further comprises a fin and a gate dielectric layer between said gate and said fin, wherein said second dielectric layer has less leakage than said gate dielectric.

9. The device of claim 5, wherein said substrate has an upwardly-facing first surface at an upper level and an upwardly-facing second surface at a lower level, said first dielectric layer being a dielectric layer formed on said first surface, said second dielectric layer being a dielectric layer formed on said second surface, and a fin of said FinFET is formed over said buried layer.

10. The device of claim 9, wherein said first dielectric layer is a buried oxide layer and said second dielectric layer is a thin oxide layer.

11. The device of claim 1, wherein said first dielectric layer is a buried oxide layer and said second dielectric layer is a thin oxide layer providing less insulating effect than said buried oxide layer, said gate being capacitively coupled to said substrate.

12. The device of claim 1, wherein said device further comprises a fin and a gate dielectric layer between said gate and said fin, wherein said second dielectric layer has less leakage than said gate dielectric.

13. The device of claim 1, wherein said substrate has an upwardly-facing first surface at an upper level and an upwardly-facing second surface at a lower level,

said first dielectric layer being a dielectric layer formed on said first surface, said second dielectric layer being a thin dielectric layer formed on said second surface, and a fin of said FinFET being formed over said buried layer.

14. The device of claim 12, wherein said first dielectric layer is a buried oxide layer and said second dielectric layer is a thin oxide layer.